FIG. 1

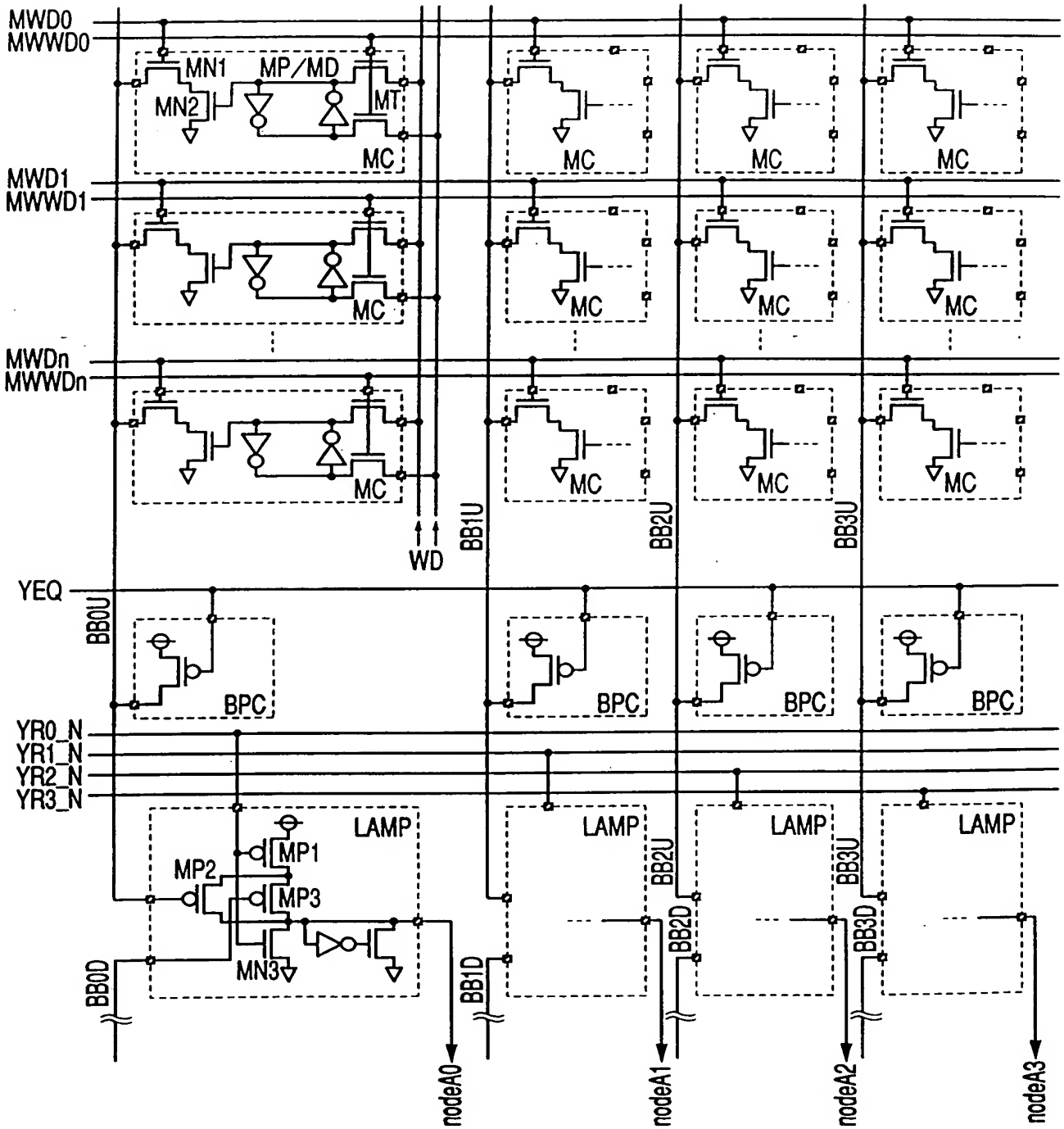

MWD0
MWWD0
MWD1
MWWD1
MWDn
MWWDn
MN1
MP/MD
MN2
MT
MC
WD
BB1U
BB2U
BB3U
YEQ
BB0U
BPC
YR0_N
YR1_N
YR2_N
YR3_N
LAMP
MP1
MP2
MP3
MN3
BB0D
BB1D
BB2D
BB3D
nodeA0
nodeA1
nodeA2
nodeA3

FIG. 2

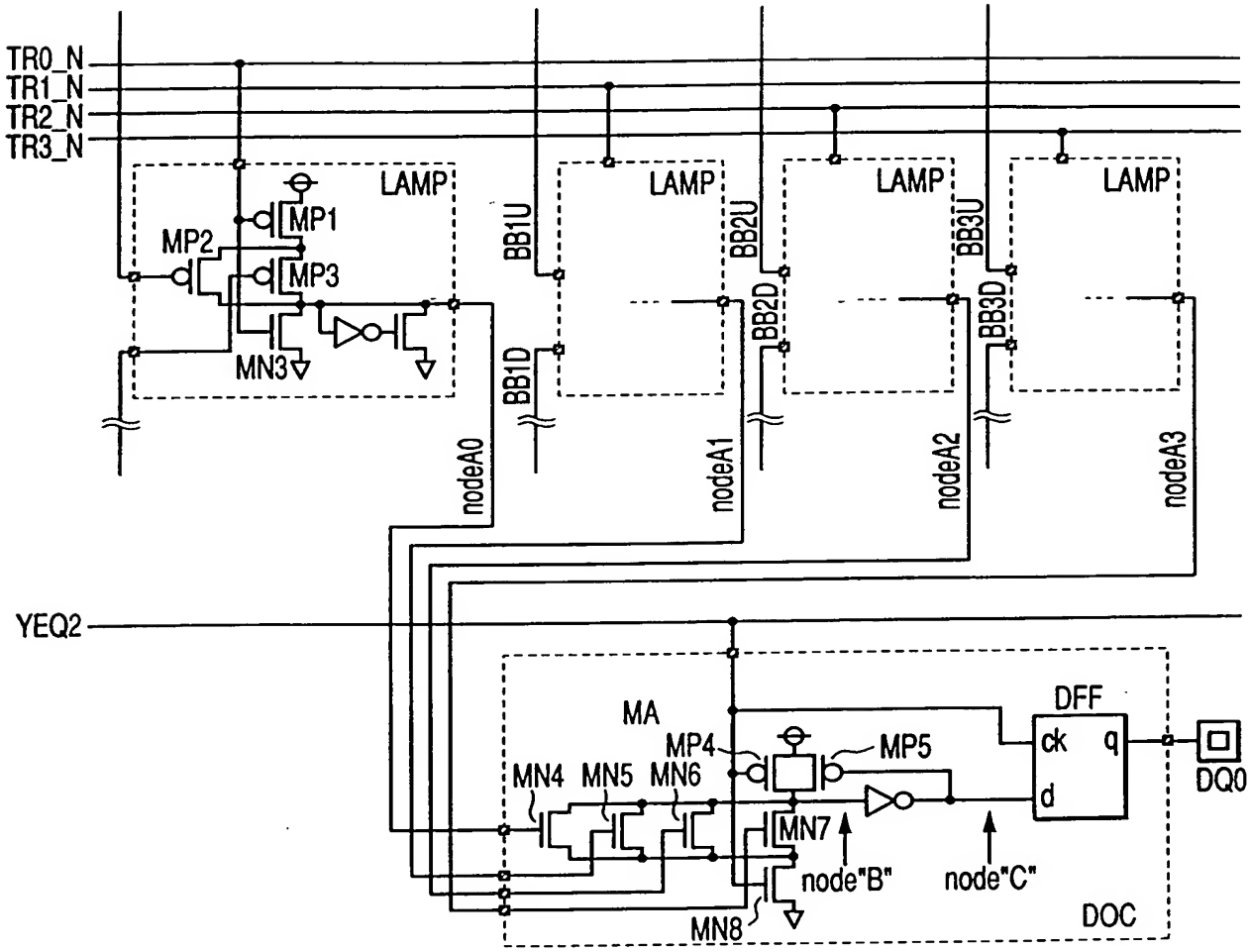

TR0_N
TR1_N
TR2_N
TR3_N
LAMP
LAMP
LAMP
LAMP
MP1
MP2
MP3
MN3
BB1U
BB1D
BB2U
BB2D
BB3U
BB3D
nodeA0
nodeA1
nodeA2
nodeA3
YEQ2
MA
MP4
MP5
MN4
MN5
MN6
MN7
MN8
node"B"
node"C"
DFF
ck
q
d
DQ0
DOC

FIG. 3

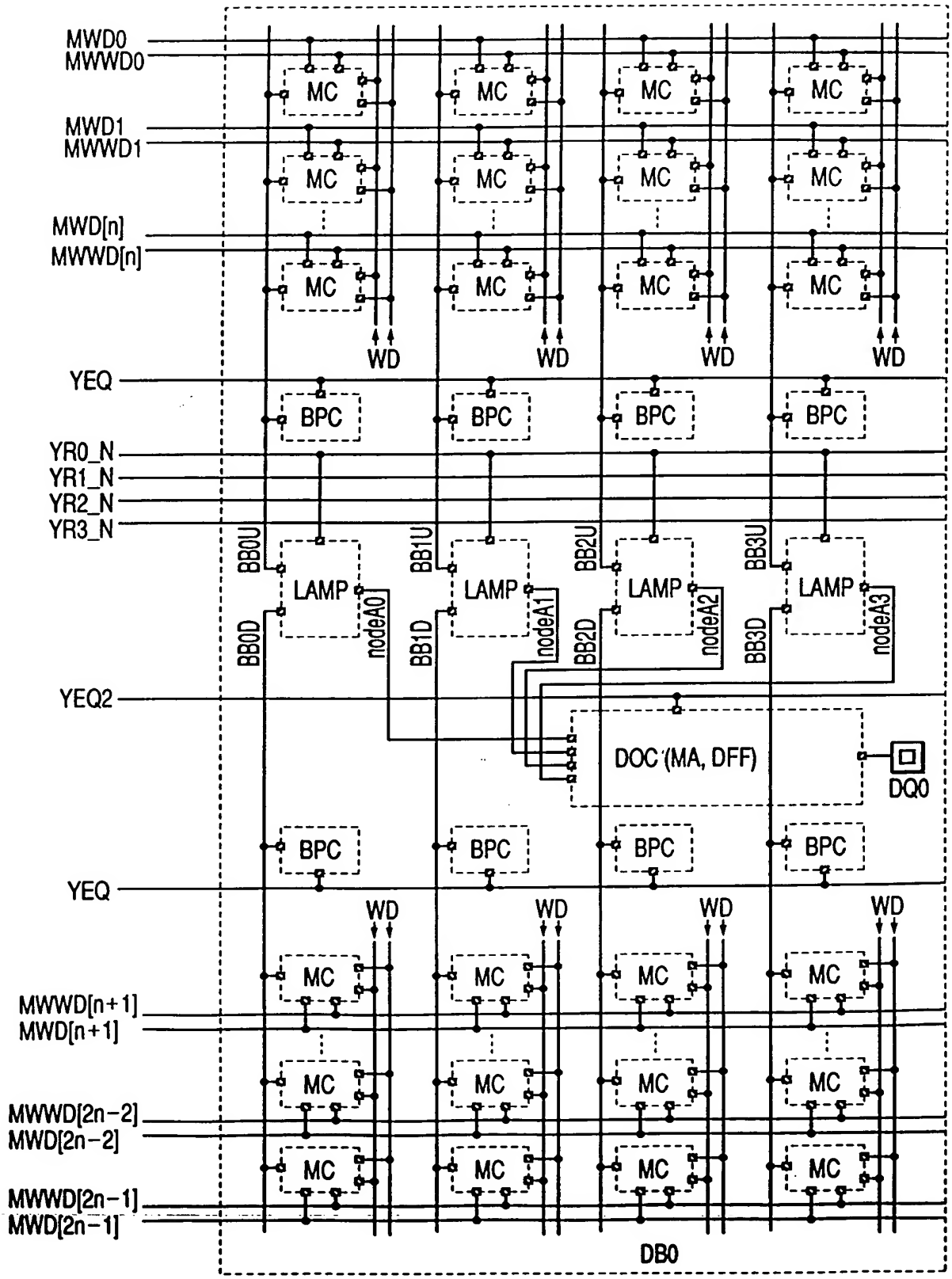

MWD0
MWWD0
MWD1
MWWD1
MWD[n]
MWWD[n]
MC
WD
YEQ
BPC
YR0_N
YR1_N
YR2_N
YR3_N
BB0U
BB1U
BB2U
BB3U
LAMP
BB0D
BB1D
BB2D
BB3D
nodeA0
nodeA1
nodeA2
nodeA3
YEQ2
DOC (MA, DFF)
DQ0
YEQ
MWWD[n+1]
MWD[n+1]
MWWD[2n-2]
MWD[2n-2]
MWWD[2n-1]
MWD[2n-1]
DB0

FIG. 4

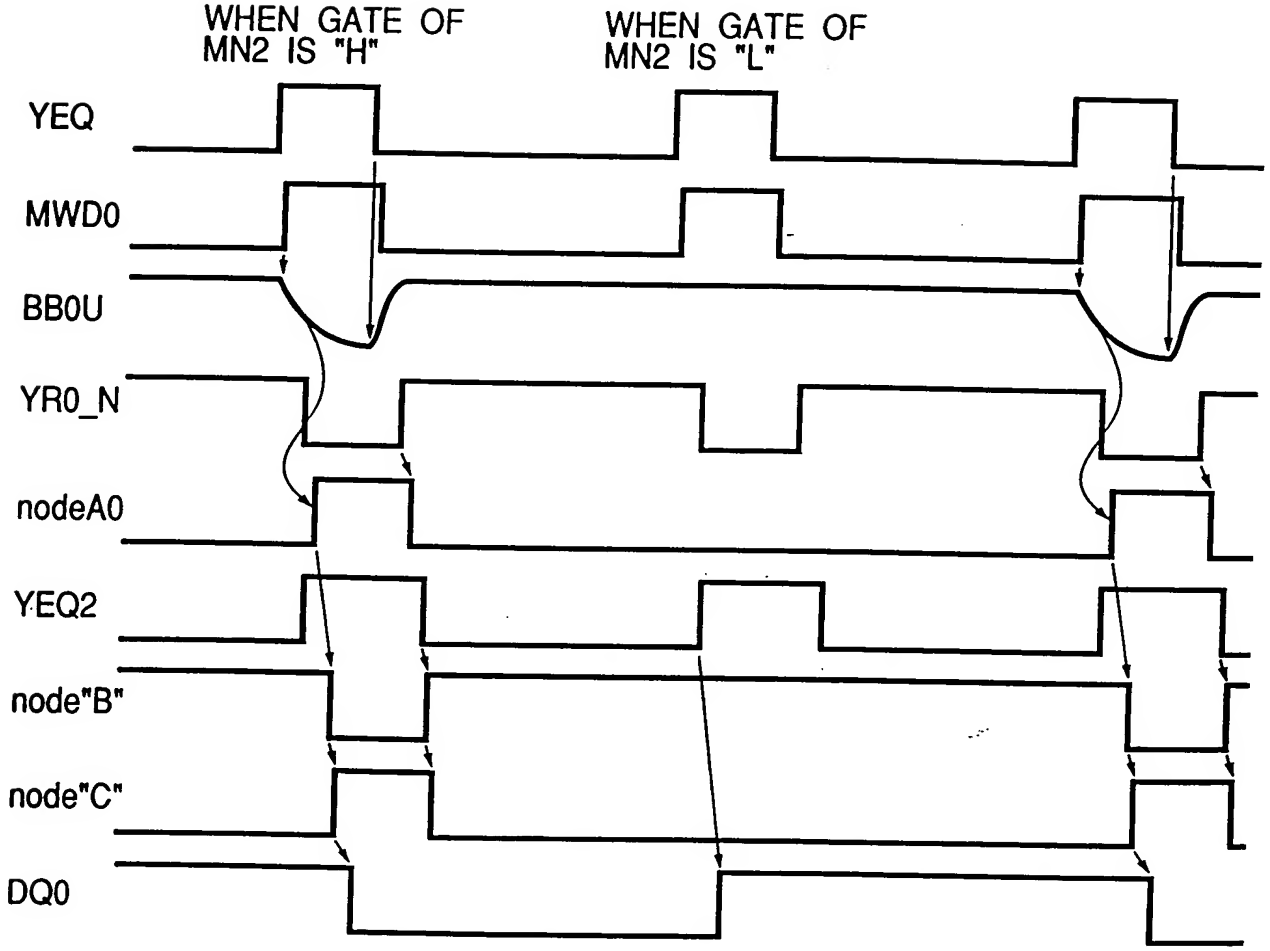
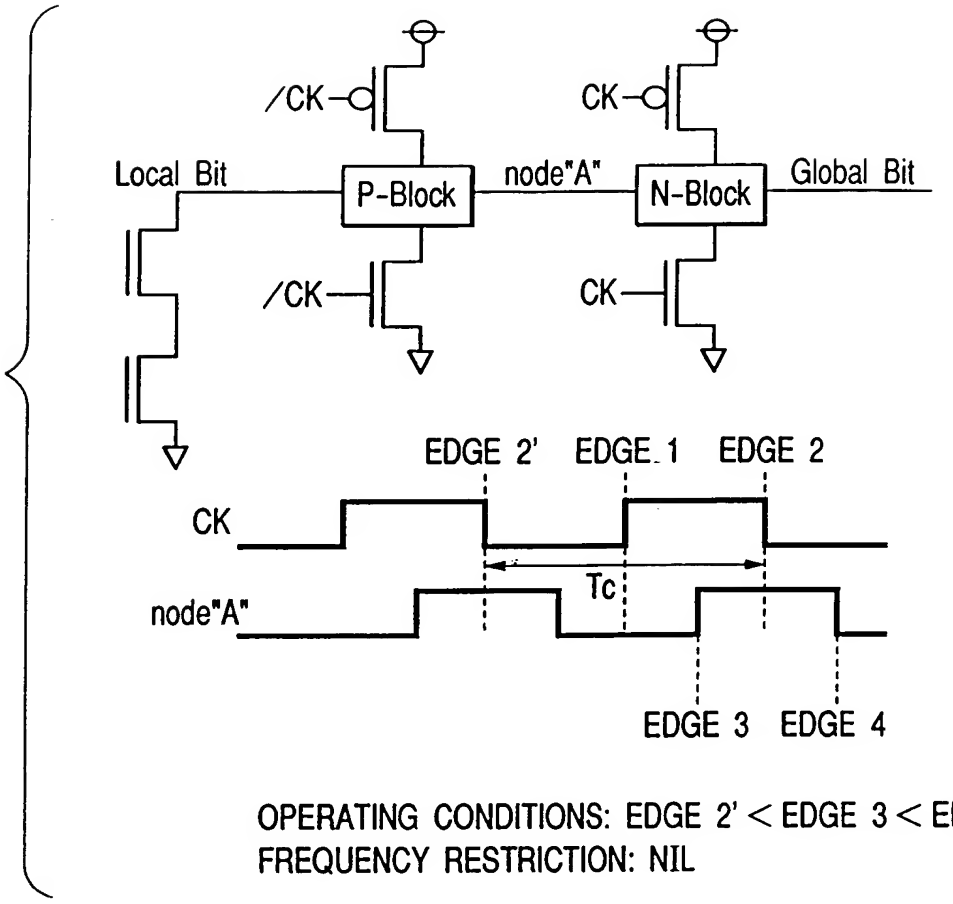
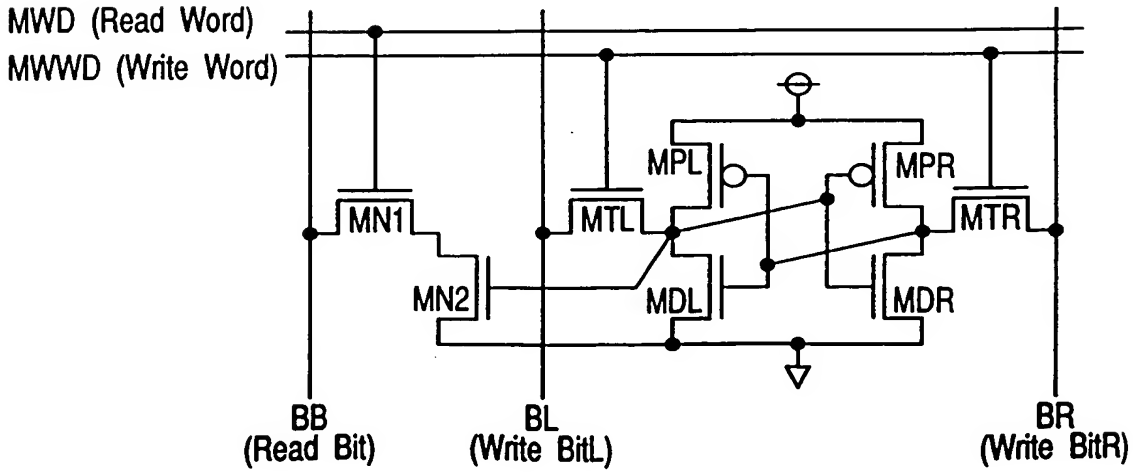

WHEN GATE OF MN2 IS "H"
WHEN GATE OF MN2 IS "L"
YEQ
MWD0
BB0U
YR0_N
nodeA0
YEQ2
node"B"
node"C"
DQ0

FIG. 5



OPERATING CONDITIONS: EDGE 2' < EDGE 3 < EDGE 2
FREQUENCY RESTRICTION: NIL

FIG. 6



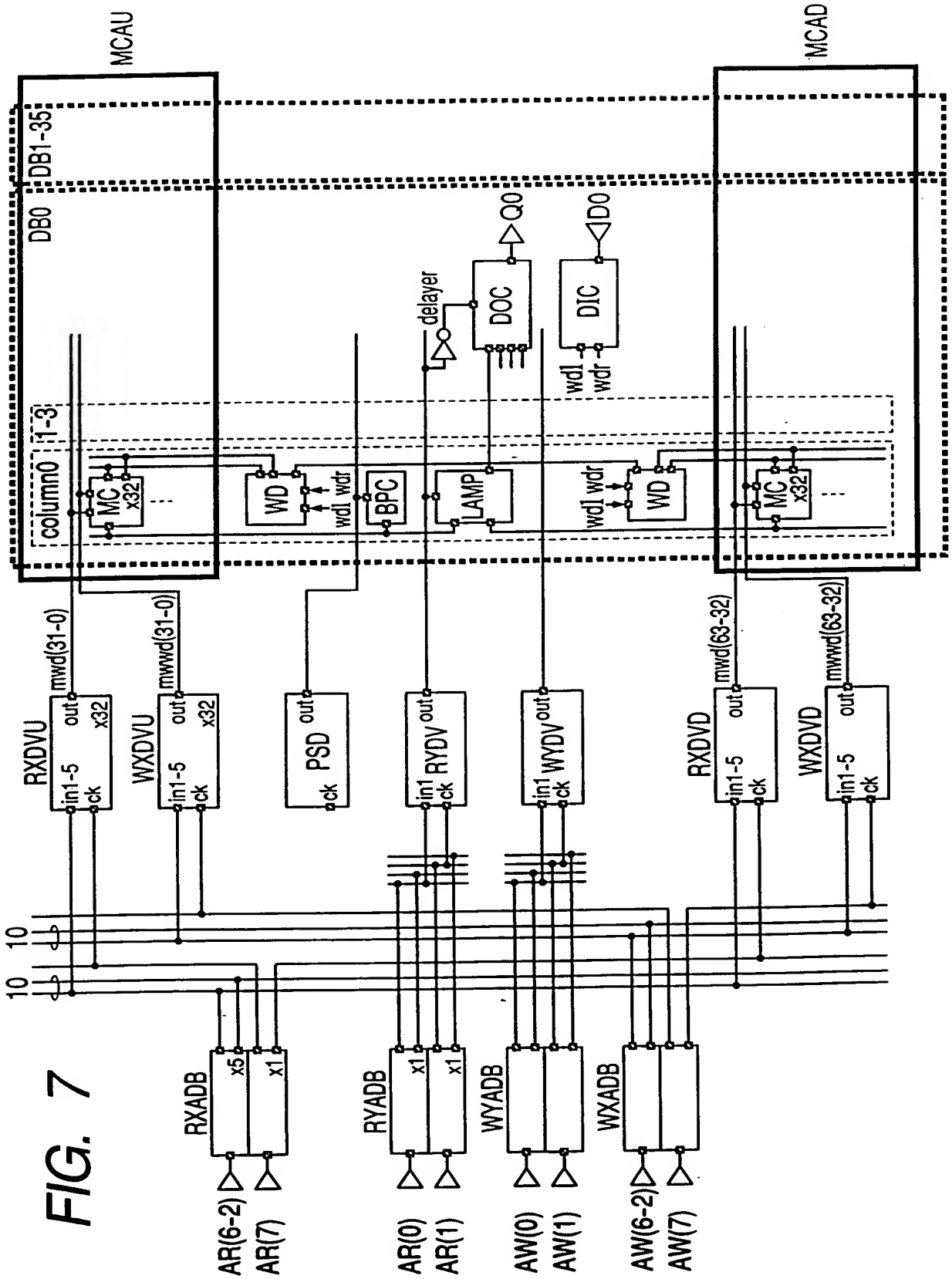

MCAU
MCAD
DB1-35
DB0
1-3
column0
MC
x32
WD
wdl wdr
BPC
LAMP
delayer
DOC
DIC
Q0
D0
wdl
wdr
mwd(31-0)
mwwd(31-0)
mwd(63-32)
mwwd(63-32)
RXDVU
WXDVU
PSD
RYDV
WYDV
RXDVD
WXDVD
in1-5
in1
ck
out
10
RXADB
RYADB
WYADB
WXADB
x5
x1
AR(6-2)
AR(7)
AR(0)
AR(1)
AW(0)
AW(1)
AW(6-2)
AW(7)

FIG. 7

FIG. 8

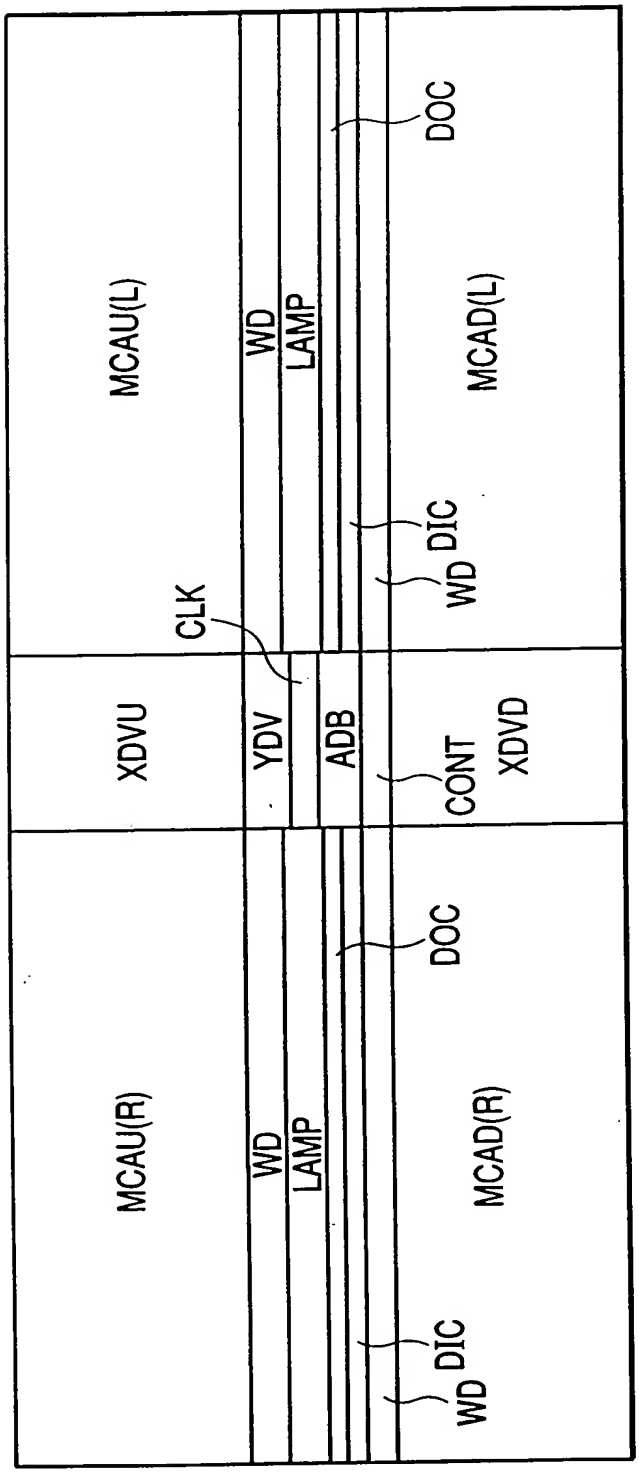

MCAU(L)
WD
LAMP
DOC
MCAD(L)
CLK
WD
DIC
XDVU
YDV
ADB
CONT
XDVD
MCAU(R)
WD
LAMP
DOC
MCAD(R)
WD
DIC

FIG. 9

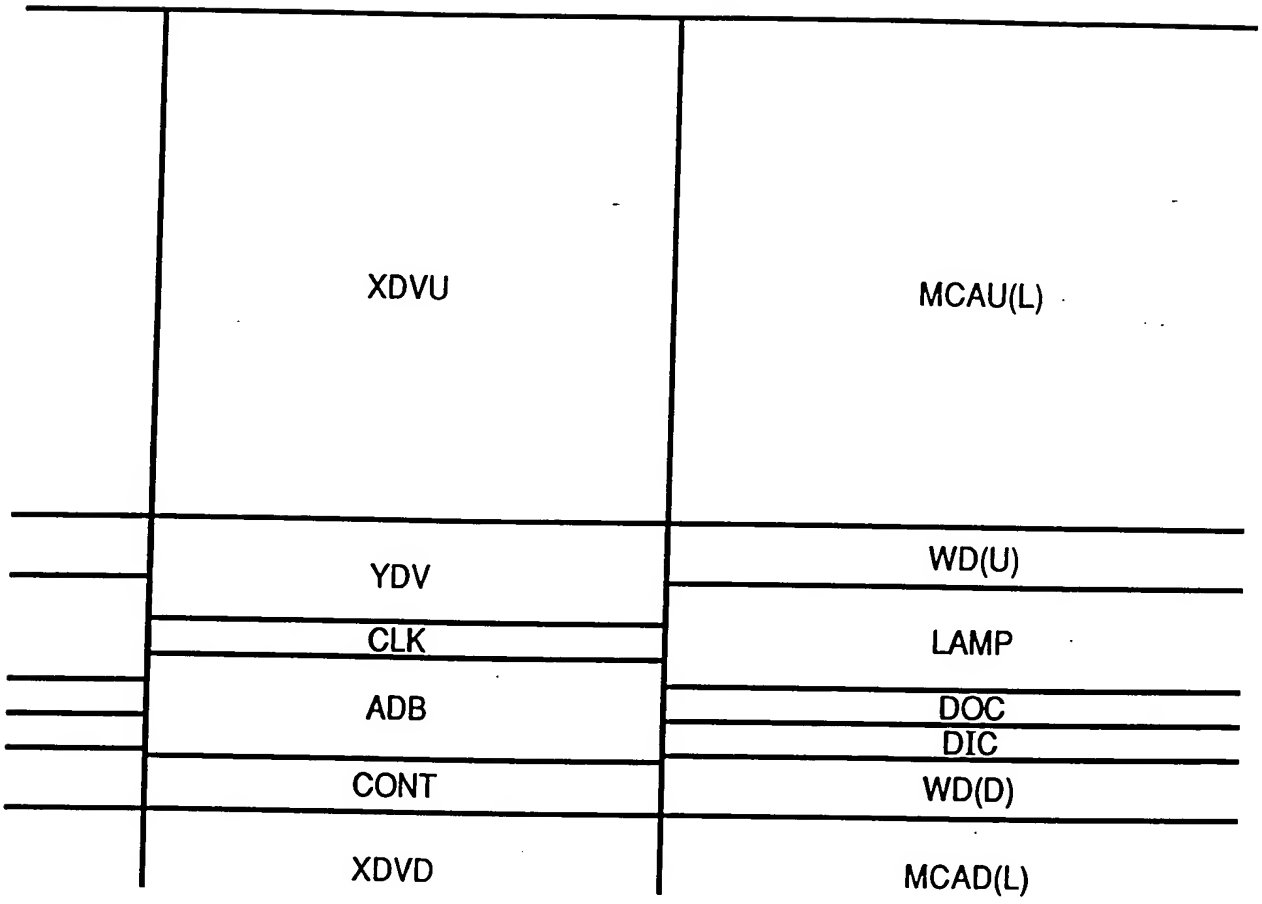


FIG. 10

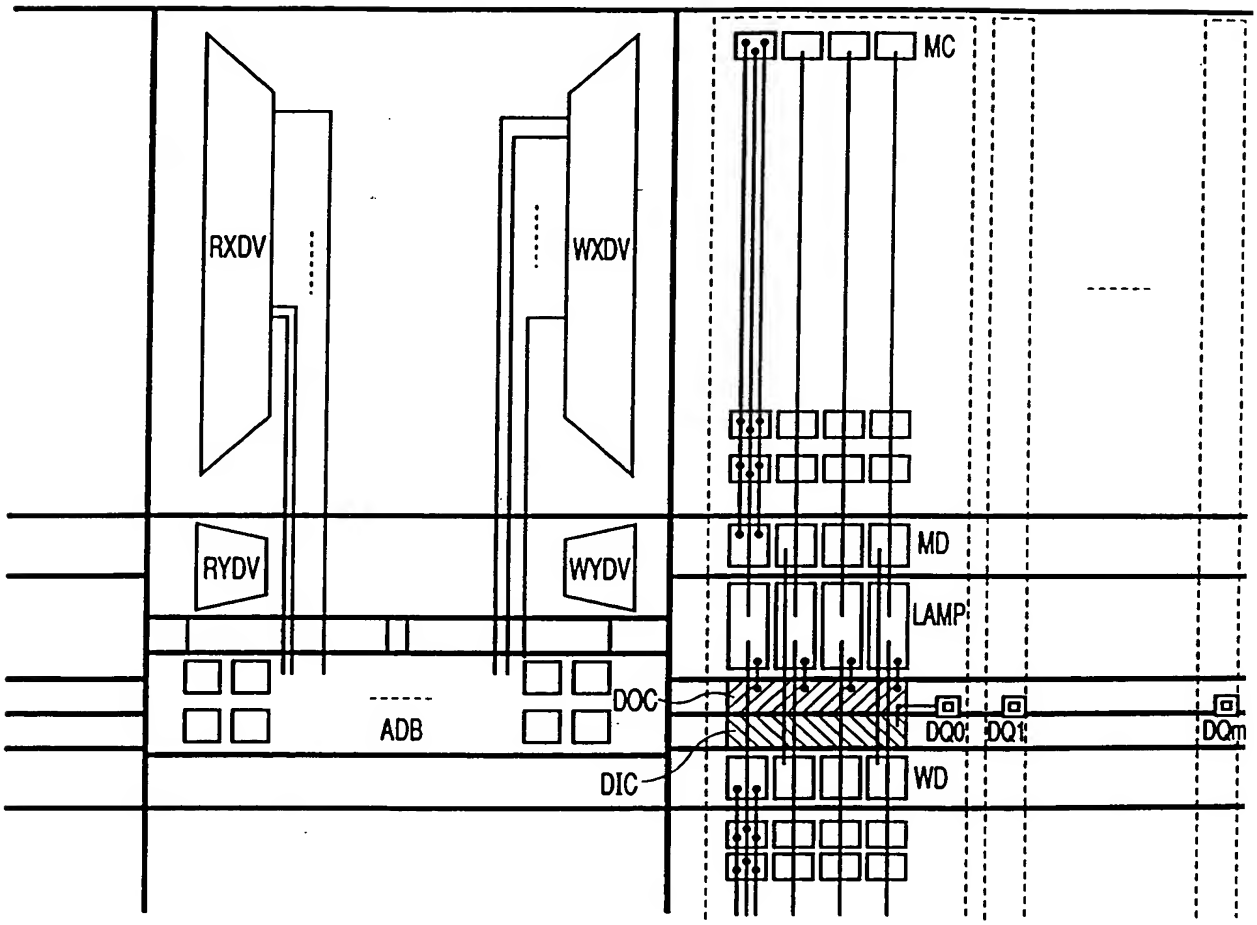


FIG. 11

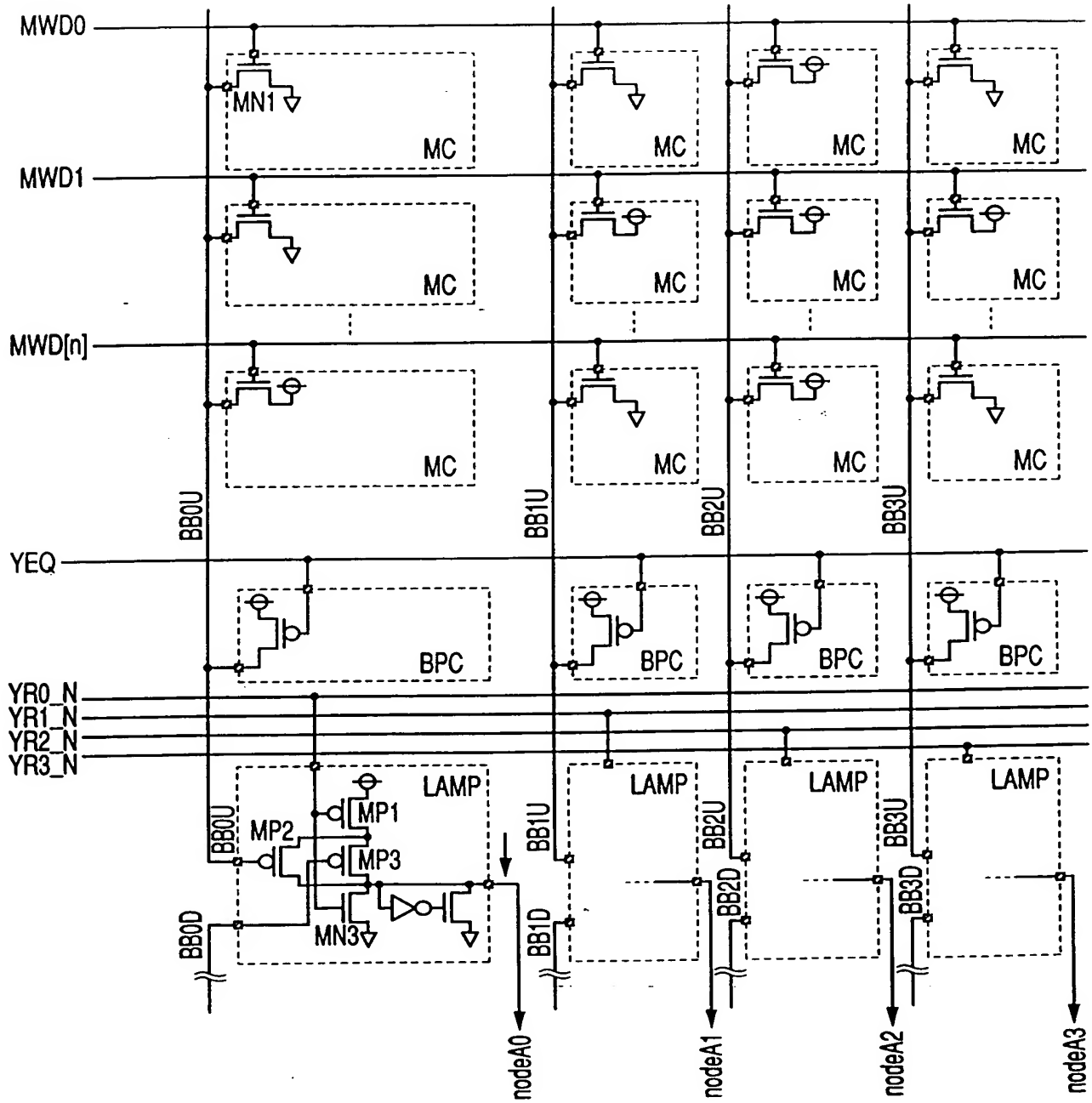

MWD0
MWD1
MWD[n]
YEQ
YR0_N
YR1_N
YR2_N
YR3_N
MN1
MC
BPC
LAMP
MP1
MP2
MP3
MN3
BB0U
BB1U
BB2U
BB3U
BB0D
BB1D
BB2D
BB3D
nodeA0
nodeA1
nodeA2
nodeA3

FIG. 12

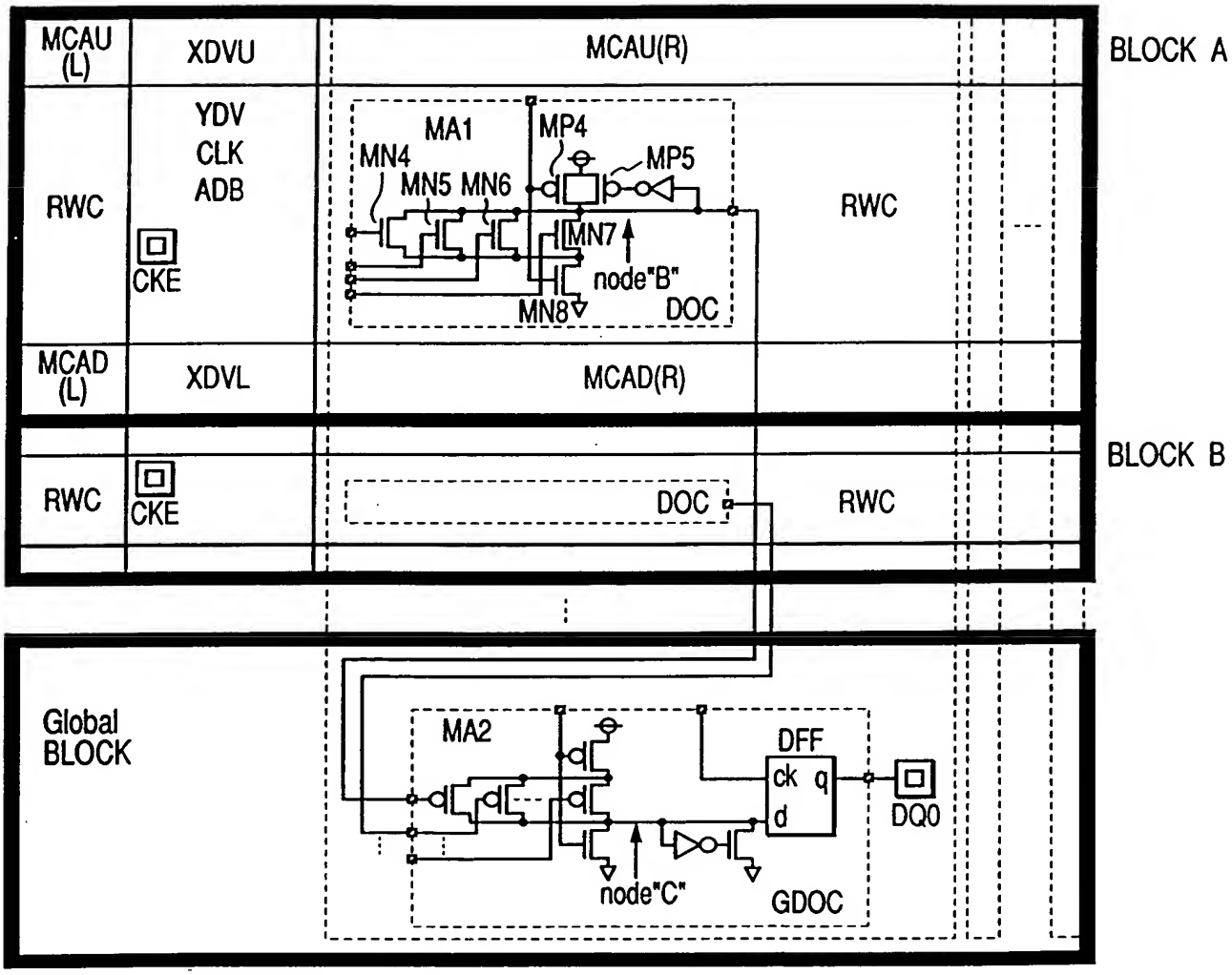

MCAU (L)
XDVU
MCAU(R)
BLOCK A
YDV
CLK
ADB
RWC
MA1
MP4
MN4
MP5
MN5 MN6
RWC
MN7
CKE
node"B"
MN8
DOC
MCAD (L)
XDVL
MCAD(R)
BLOCK B
RWC
CKE
DOC
RWC
Global BLOCK
MA2
DFF
ck q
d
DQ0
node"C"
GDOC

FIG. 13

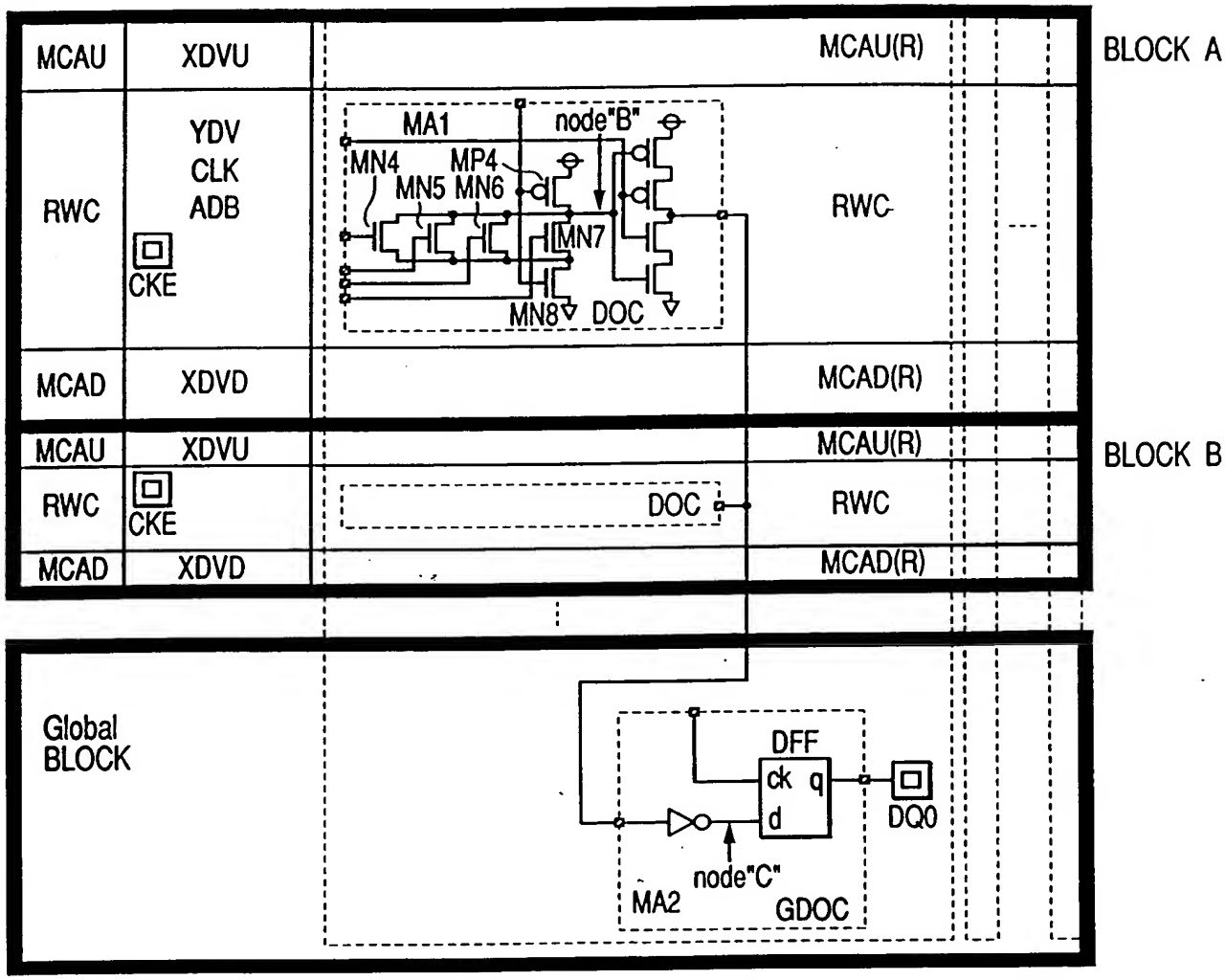

MCAU
XDVU
MCAU(R)
BLOCK A
RWC
YDV
CLK
ADB
CKE
MA1
node"B"
MN4
MP4
MN5 MN6
MN7
MN8
DOC
RWC
MCAD
XDVD
MCAD(R)
MCAU
XDVU
MCAU(R)
BLOCK B
RWC
CKE
DOC
RWC
MCAD
XDVD
MCAD(R)
Global
BLOCK
DFF
ck q
d
DQ0
node"C"
MA2
GDOC

FIG. 14

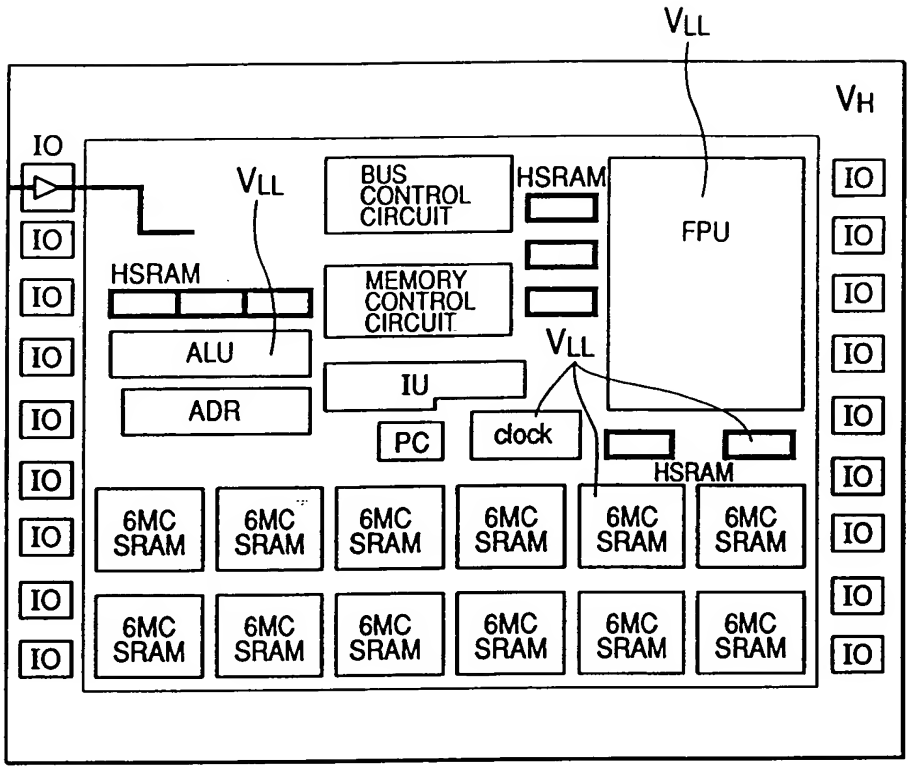

VLL
VH
IO
VLL
BUS CONTROL CIRCUIT
HSRAM
FPU
HSRAM
MEMORY CONTROL CIRCUIT
ALU
VLL
IU
ADR
PC
clock
HSRAM
6MC SRAM
6MC SRAM
6MC SRAM
6MC SRAM
6MC SRAM
6MC SRAM
6MC SRAM
6MC SRAM
6MC SRAM
6MC SRAM
6MC SRAM
6MC SRAM

FIG. 15

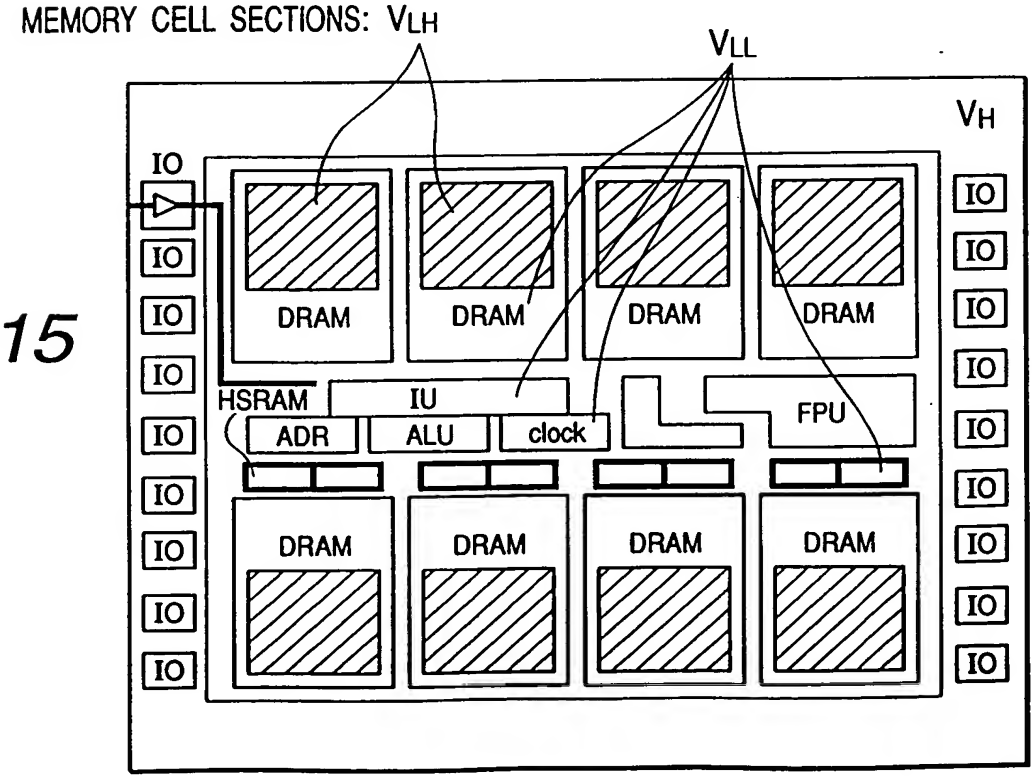

MEMORY CELL SECTIONS: VLH
VLL
VH
IO
DRAM
DRAM
DRAM
DRAM
HSRAM
IU
FPU
ADR
ALU
clock
DRAM
DRAM
DRAM
DRAM

FIG. 16

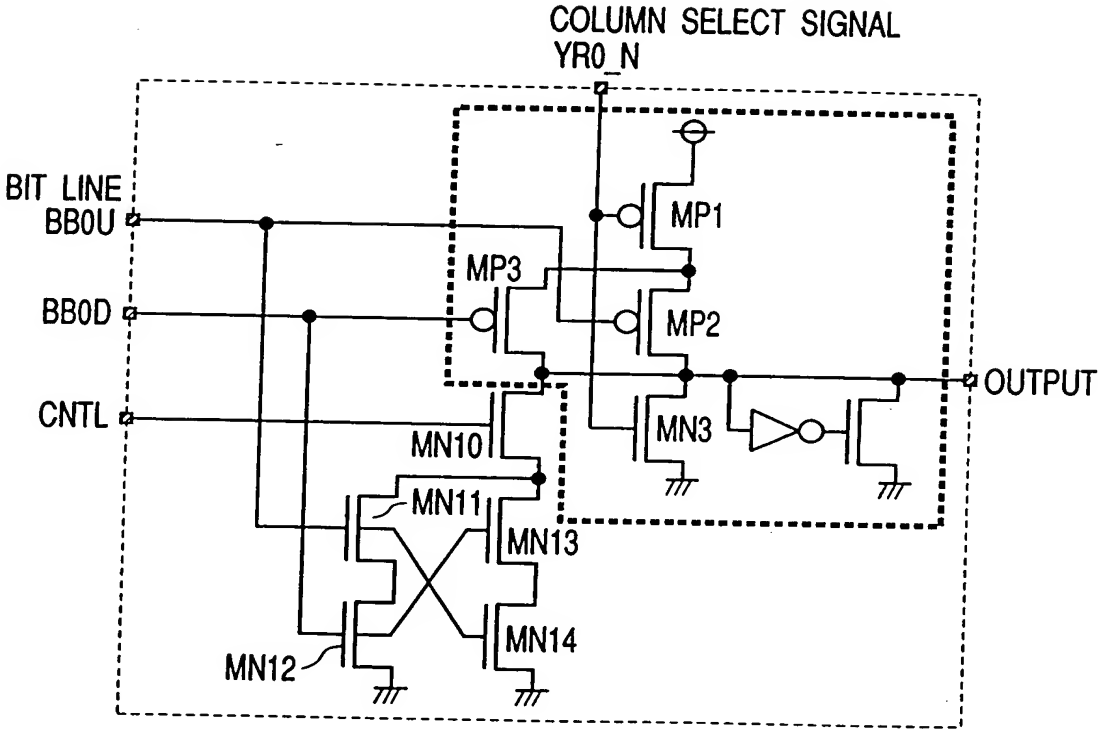

COLUMN SELECT SIGNAL
YR0_N
BIT LINE
BB0U
BB0D
CNTL
MP1
MP3
MP2
MN3
MN10
MN11
MN13
MN14
MN12
OUTPUT

FIG. 17

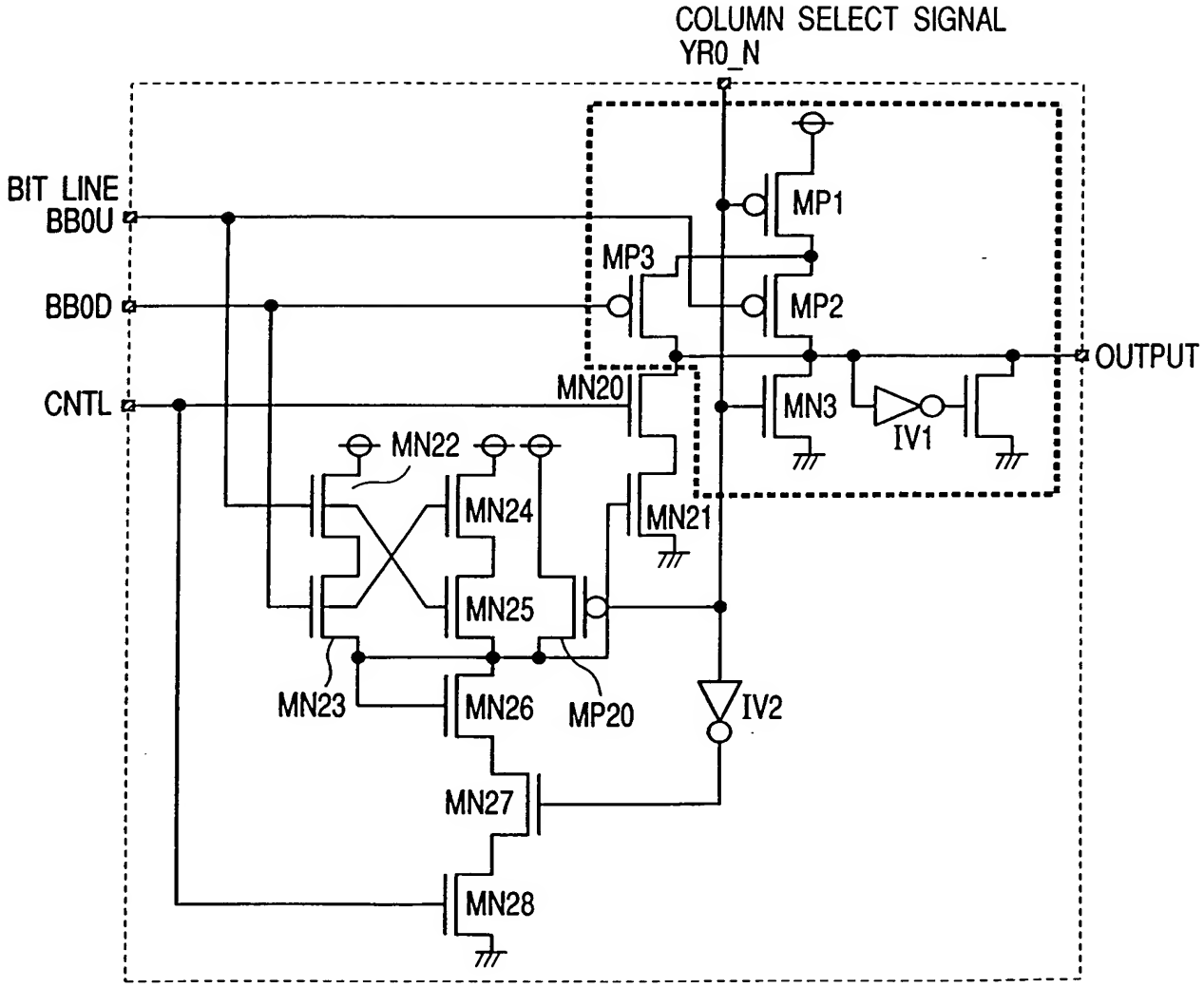
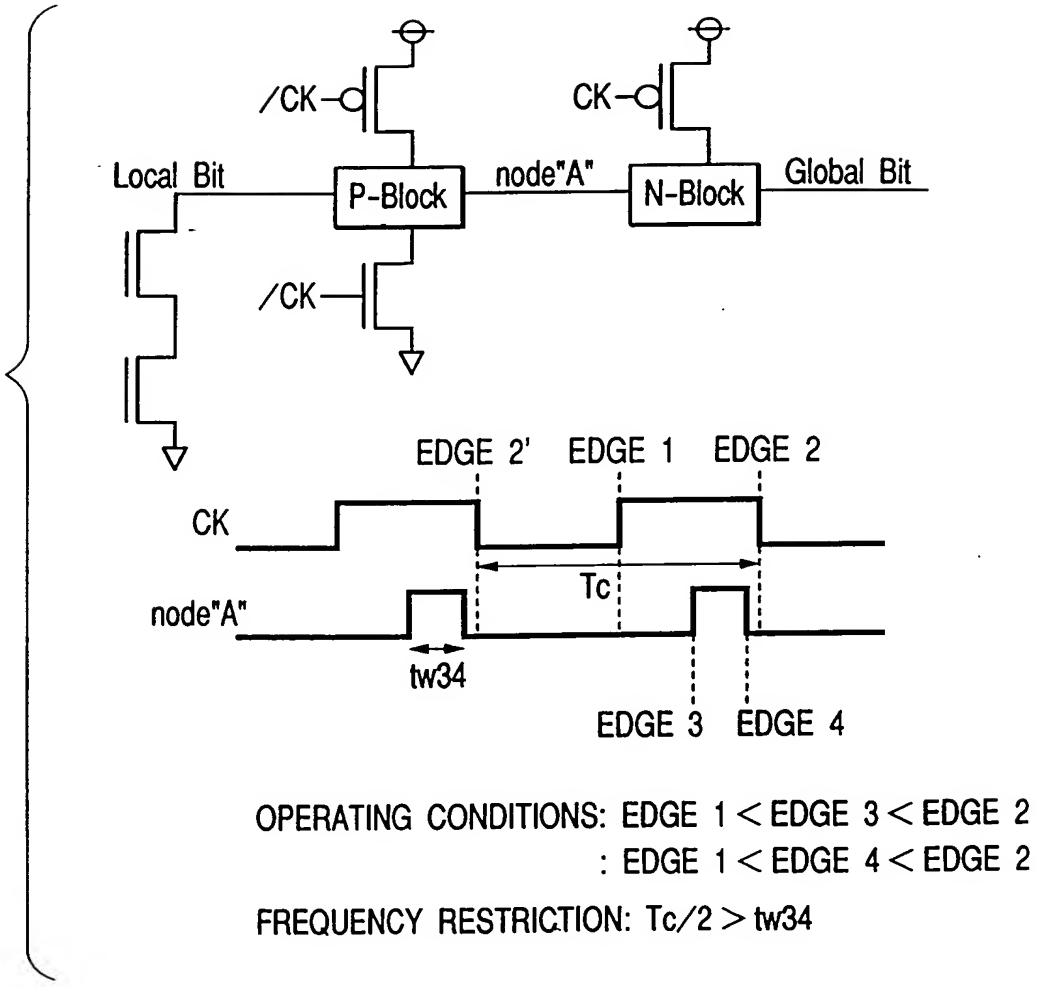

COLUMN SELECT SIGNAL
YR0_N
BIT LINE
BB0U
BB0D
CNTL
MP1
MP3
MP2
OUTPUT
MN20
MN3
IV1
MN22
MN24
MN21
MN25
MN23
MN26
MP20
IV2
MN27
MN28

FIG. 18



OPERATING CONDITIONS: EDGE 1 < EDGE 3 < EDGE 2
: EDGE 1 < EDGE 4 < EDGE 2

FREQUENCY RESTRICTION: Tc/2 > tw34